6.2.1 Synthesis of Mixed Control-Dataflow Systems 149
6.2.2 System-level Low Power Synthesis 150
6.2.3 Smart Frameworks.....150

7 REFERENCES.....152

8 APPENDIX.....162

A1 ILP Formulation for Problem P1 162
A2 Proof of NP-Completeness for Problem P1 166
A3 ILP formulation for Problem P2 167
A4 Complexity Analysis of the GCLP Algorithm 172
A5 Complexity Analysis of the Bin Selection Procedure 174
A6 Complexity Analysis of the MIBS Algorithm 175
A7 Algorithm for Random Graph Generation 176
A7.1 Random DAG Generation 176
A7.2 Generation of Hardware-Software Area-Time Values 177
A7.3 Implementation Curve Generation 181
A8 Estimation of Area and Execution Time Parameters 182
A8.1 Hardware Estimation 182
A8.2 Software Estimation 184
A9 Automated Flow Execution in the DMM Domain 185
A9.1 Preliminaries 185
A9.2 Run All mode 186
A9.3 Run Upto mode 193
A9.4 Run This mode 193

4.1.2 The Cosynthesis Approach 90
4.1.3 Hardware Synthesis 95
4.1.4 Software Synthesis 99
4.1.5 Interface Synthesis 101
4.1.6 Other Synthesis Approaches 103
4.1.7 Summary 104
4.2 Cosimulation 105
4.2.1 The Ptolemy Framework 109
4.2.2 Cosimulation Using Ptolemy 113
4.2.2.1 System-level Modeling 114
4.2.2.2 System Simulation 116

5 DESIGN SPACE EXPLORATION 118
5.1 Related Work 120
5.2 Design Methodology Management: Requirements 122
5.3 Infrastructure 124
5.3.1 Flow, Tool, and Data Model 124
5.3.2 Dependencies 127
5.3.3 Flow Management 128
5.4 Implementation: DMM Domain within Ptolemy 129
5.5 Examples 133
5.5.1 Multiprocessor System Design 134
5.5.2 Design Assistant 136
5.6 Summary 141

6 CONCLUSION 143
6.1 Contribution 143
6.1.1 Partitioning 145
6.1.2 Cosynthesis and Cosimulation 147
6.1.3 Design Methodology Management 148
6.2 Future directions 149

3.3 The Binary Partitioning Problem: GCLP Algorithm 37
3.3.1 Algorithm Foundation 37
3.3.2 Global Criticality (GC) 41
3.3.3 Local Phase (LP) 44
3.3.3.1 Motivation for Local Phase Classification 44
3.3.3.2 Local Phase 1 or Extremity nodes 46
3.3.3.3 Local Phase 2 or Repeller Nodes 49
3.3.3.4 Local Phase 3 or Normal Nodes 52
3.3.4 GCLP Algorithm 53
3.4 Performance of the GCLP Algorithm 56
3.4.1 Examples 56
3.4.2 Experiment 1: GCLP vs. ILP 58
3.4.3 Experiment 2: GCLP with and without local phase nodes 60
3.4.4 Algorithm Trace 61
3.4.5 Summary of the GCLP algorithm 65
3.5 Algorithm for Extended Partitioning: Design Objectives 66
3.6 Implementation-bin Selection 69
3.6.1 Overview 69
3.6.2 Bin Fraction Curve (BFC) 71
3.6.3 Implementation-bin Selection 73
3.7 The Extended Partitioning Problem: MIBS Algorithm 75
3.8 Performance of the MIBS Algorithm 77
3.8.1 Estimation of the Hardware Implementation Curve 77
3.8.2 Experiment 1: MIBS vs. ILP 78
3.8.3 Experiment 2: Binary Partitioning vs. Extended Partitioning 79
3.8.4 Parameter Tuning 81
3.9 Summary 82

4 COSYNTHESIS AND COSIMULATION 84

4.1 Cosynthesis 85
4.1.1 Architectural Model 85

TABLE OF CONTENTS

ABSTRACT **1**

DEDICATION ..... **iii**

LIST OF FIGURES ..... **viii**

ACKNOWLEDGEMENTS ..... **xi**

1 INTRODUCTION **1**

1.1 Issues in System-level Design 3

1.1.1 Partitioning 4

1.1.2 System Synthesis 7

1.1.3 System Simulation 9

1.1.4 Design-Space Exploration 9

1.2 The Codesign Philosophy for System-level Design 10

2 THE DESIGN ASSISTANT **12**

2.1 A Typical Codesign Flow and Tools for Codesign 14

2.2 Requirements for Design-Space Exploration 18

2.3 Specification Semantics 19

2.4 Target Architecture 21

2.5 Restrictions in the Design Assistant 23

2.6 Summary 24

3 EXTENDED PARTITIONING **25**

3.1 Problem Definition 26

3.1.1 Assumptions 27

3.1.2 Binary Partitioning 28

3.1.3 Extended Partitioning 28

3.2 Related Work 31

3.2.1 Binary Partitioning: Related Work 32

3.2.2 Extended Partitioning: Related Work 36