Cosimulating Synchronous DSP Designs with Analog RF Circuits

José Luis Pino and Khalil Kalbasi

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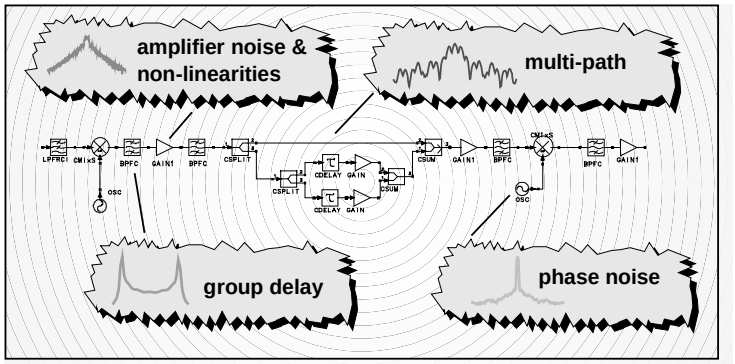
DSP designs have to work with analog and RF distortions



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What is needed in a DSP & analog RF design environment?

- Cosimulation between many different domains
  - DSP (dataflow)
  - Analog (SPICE)
  - RF (harmonic balance, Circuit Envelope)
- Natural specification syntax
- Support for both simulation and synthesis

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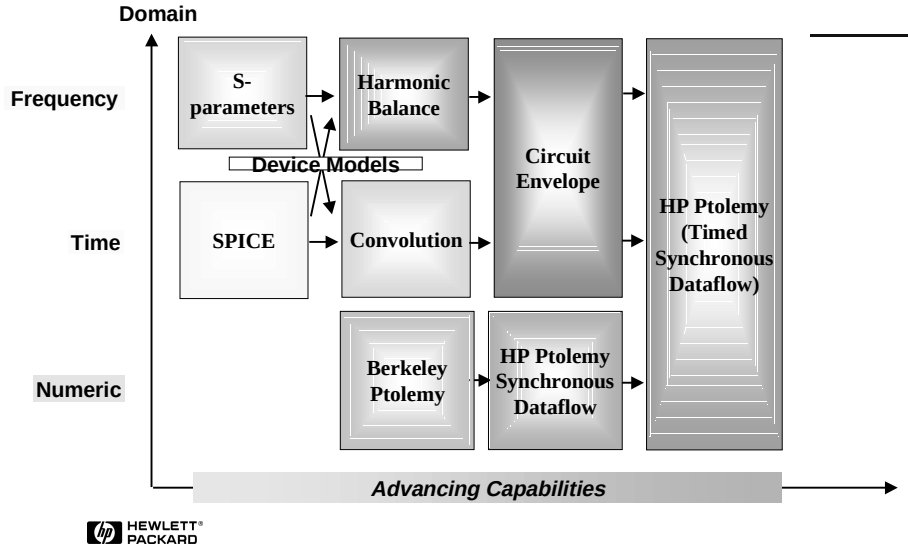
Simulation Technologies



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Dataflow problems - Synchronous dataflow solutions

- Tokens might accumulate on arcs - SDF compile time analysis guarantees bounded memory execution
- The dataflow graph might deadlock - SDF compile time analysis guarantees non-deadlocking execution
- The graph might be non-determinate - SDF is determinate by construction

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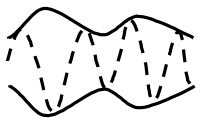
Timed Synchronous Dataflow (TSDF)

- Adds Timed data type
  - Parameters on signals are Δ_t, I, Q, f_c
- Adds Δ_t and f_c consistency checks
- Adds cosimulation with analog RF simulations
- Benefits
  - Enables modeling of RF effects to signals
  - Enables efficient RF simulations



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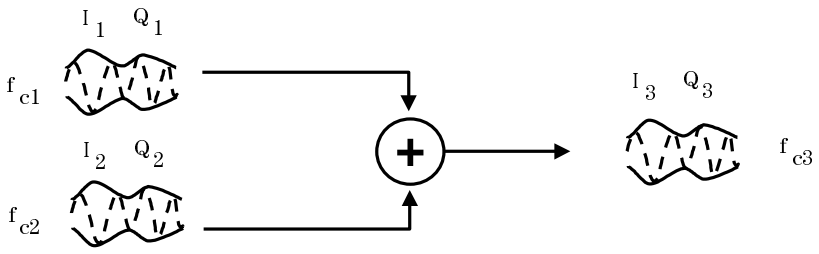
TSDF: Addition of RF signals



The sampling rate of the signals need to be sufficient to represent the envelope of the RF signals.

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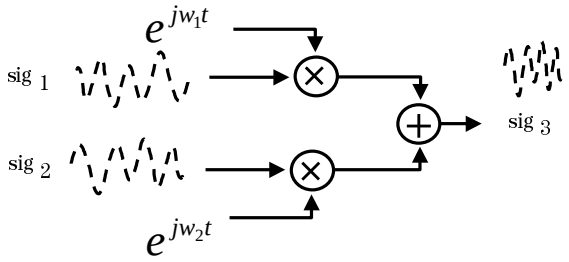
Without TSDF representation ….



The signal might need to be oversampled to fully characterize the resulting RF frequency.

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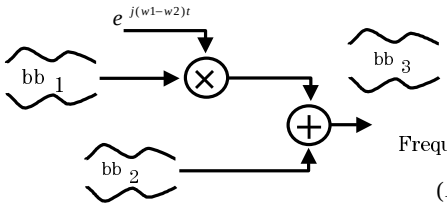
A possible workaround ….



Frequency conversion:

$$(I + jQ)e^{jw_1 t}\, e^{-jw_2}\, e^{+jw_2}$$

$$I'Q' = (I + jQ)e^{j(w1-w2)t}$$

When using complex baseband, the user has to remember the frequencies, deal with the math headaches, and implement tricks in the block diagram.

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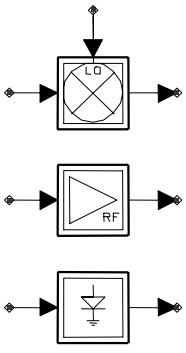
TSDF RF Modeling Technologies

- Impulse modeling of forward transmission (S21)
- High frequency nonlinearities
  - Gain compression
  - 3rd order intercept
  - Mixer intermodulation
- Propagation channel modeling
- Phase noise
- Amplifier Noise figure



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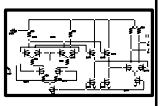
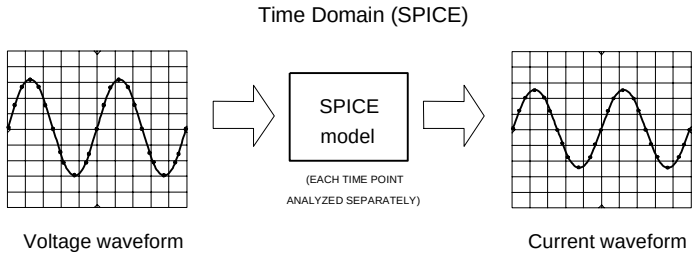
Cosimulation with linear circuit analysis tools





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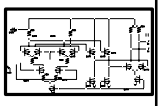
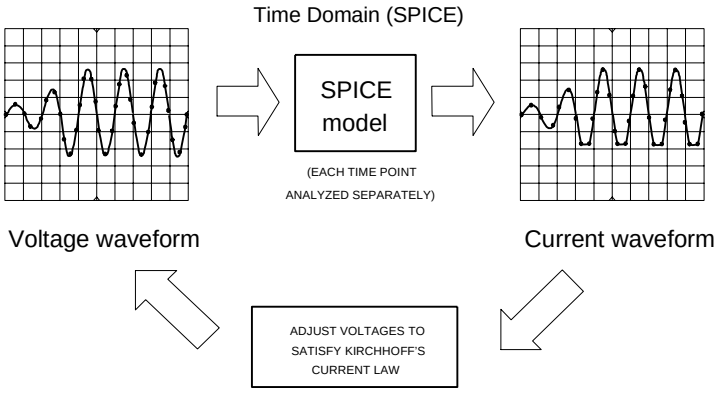
Cosimulation with nonlinear circuit analysis tools





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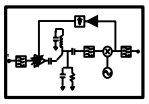
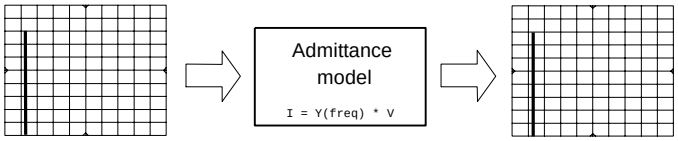
Harmonic Balance



Linear circuit analysis
in the frequency domain



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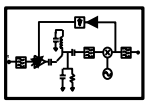
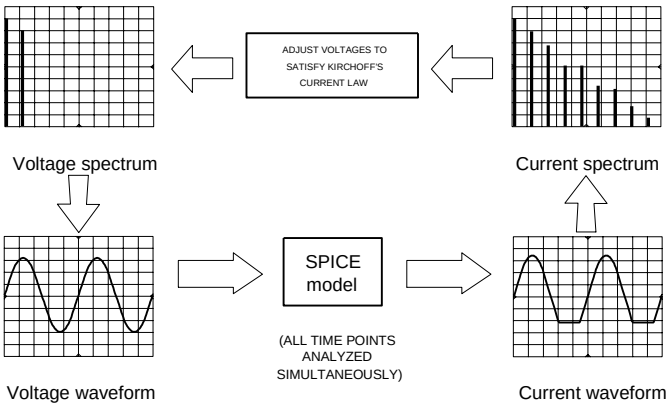
Harmonic Balance Technology



CHANGE THE VOLTAGE SPECTRUM UNTIL "KCL" IS SATISFIED AT ALL NODES

Converging toward a solution



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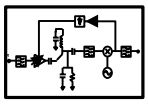
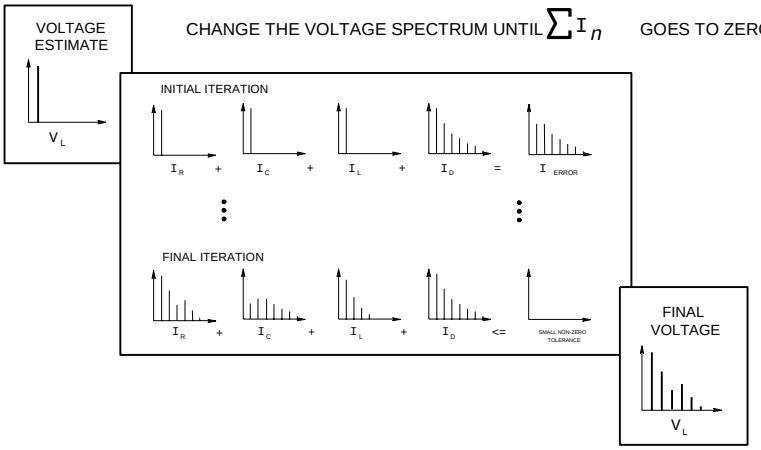
Harmonic Balance: Converging towards a solution





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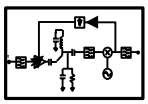
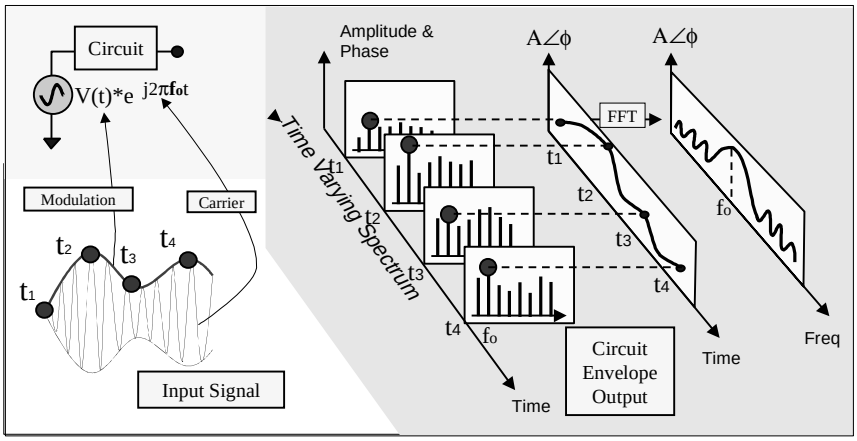
Circuit Envelope Technology





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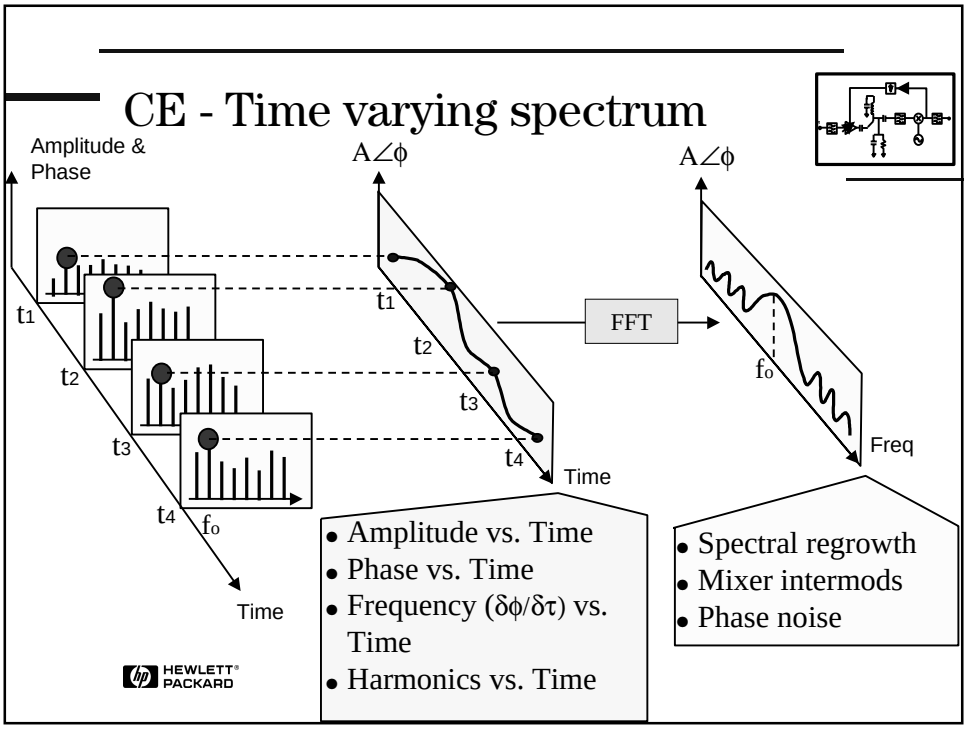
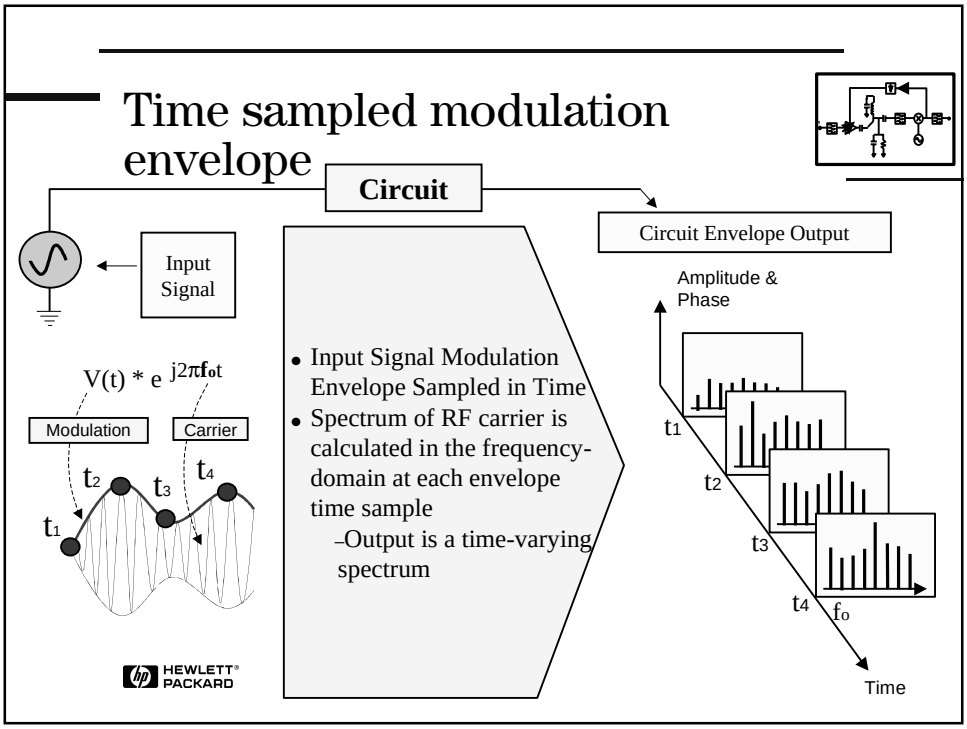
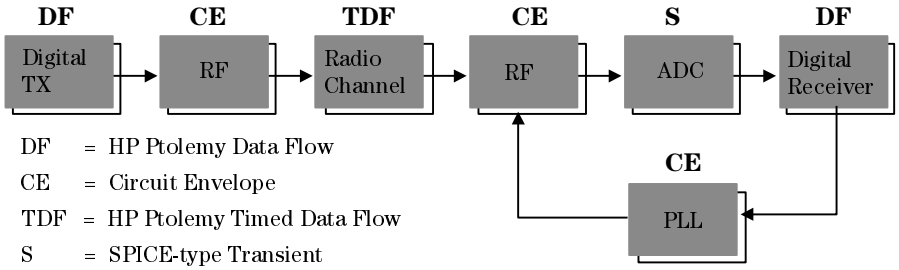




Cosimulation

- Hierarchical, heterogeneous design
- Automatic scheduling and data transfer

✓ Validation of entire design
✓ Most appropriate simulation algorithm for each section



DF = HP Ptolemy Data Flow
CE = Circuit Envelope
TDF = HP Ptolemy Timed Data Flow
S = SPICE-type Transient

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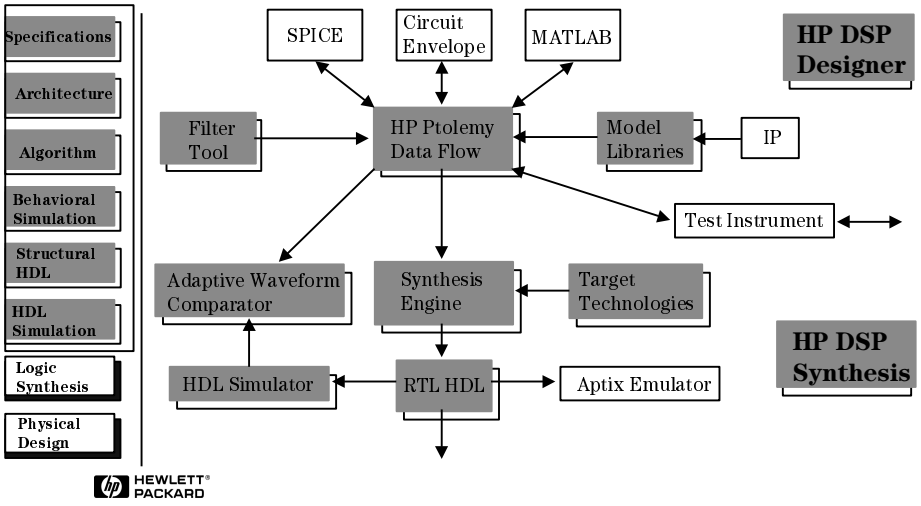
HP DSP Solutions



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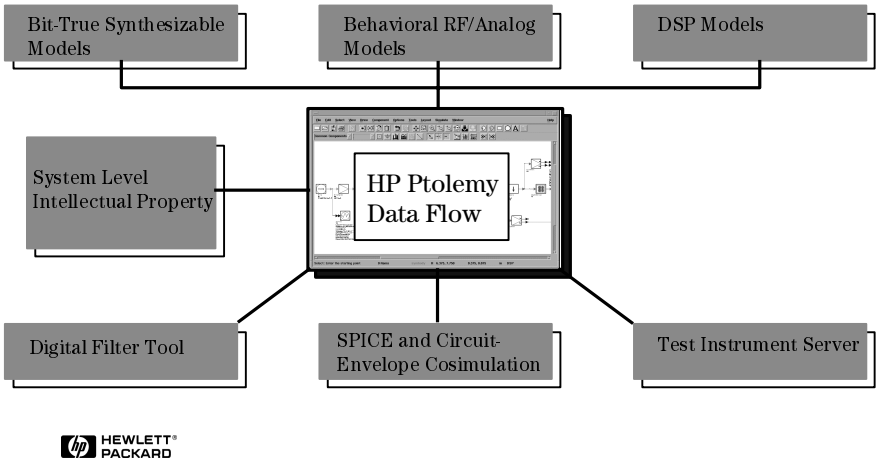
HP Ptolemy



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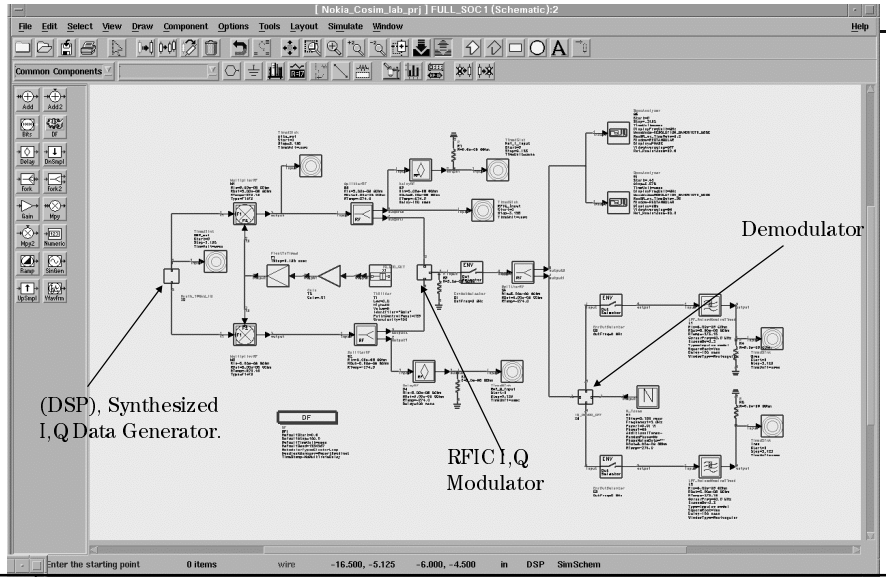
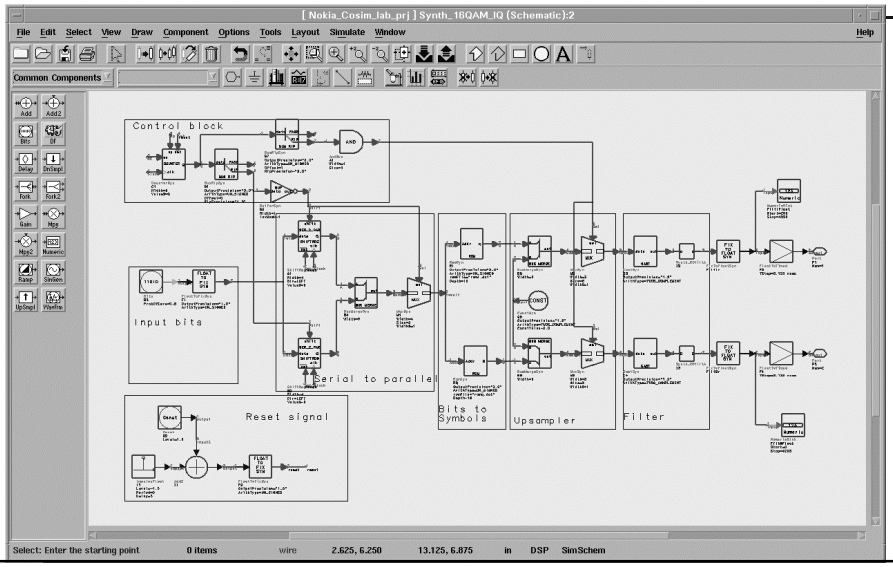
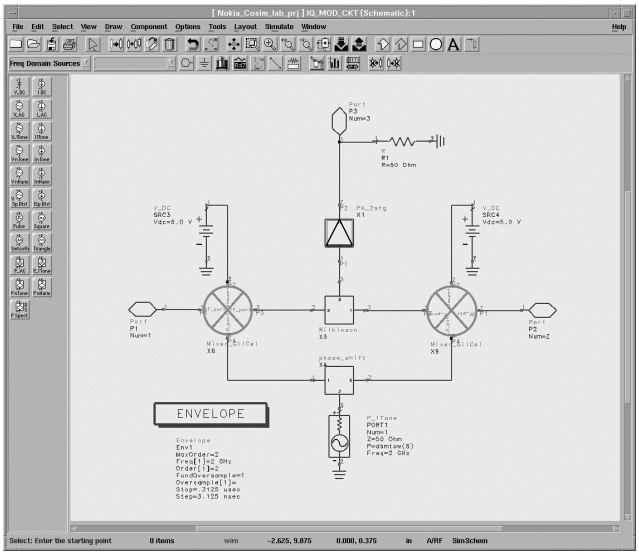
Example: 16 QAM Tx/Rx



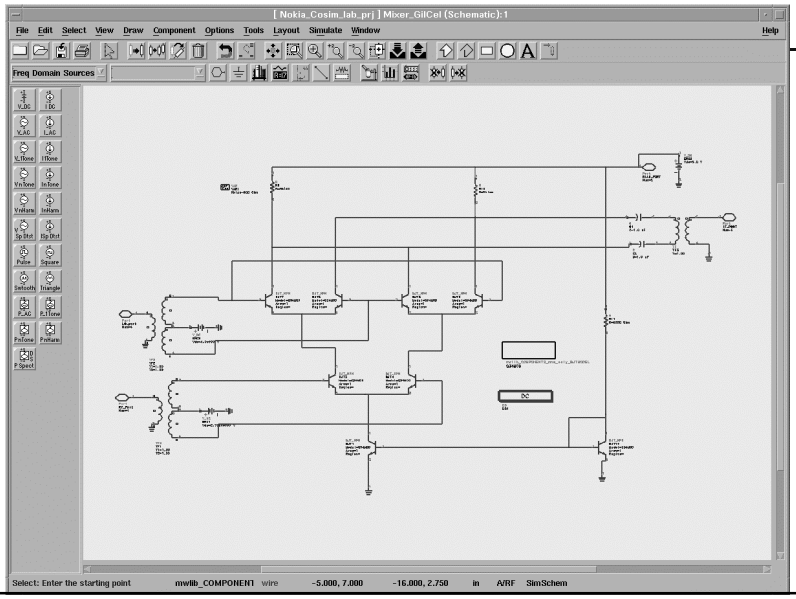
Synthesizable 16 QAM Tx



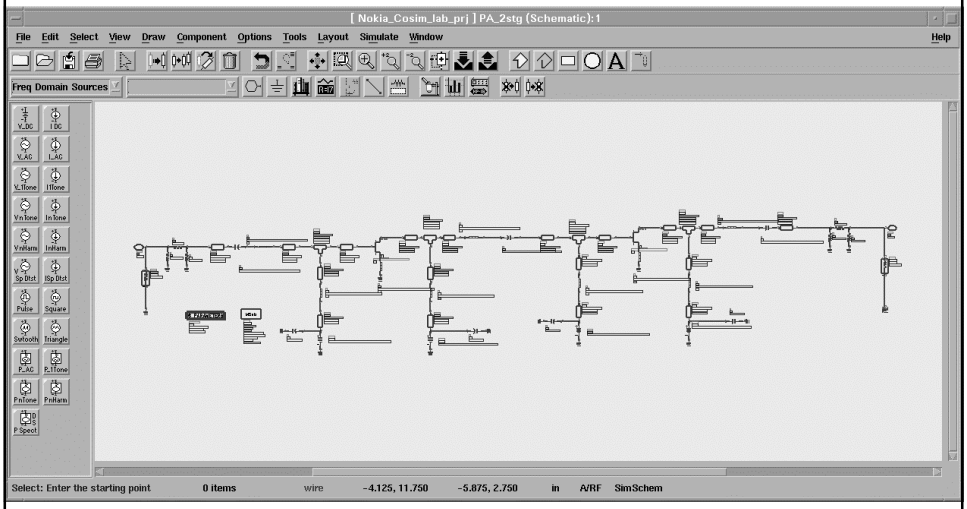
IQ Modulator



Mixer



2-Stage Power Amplifier



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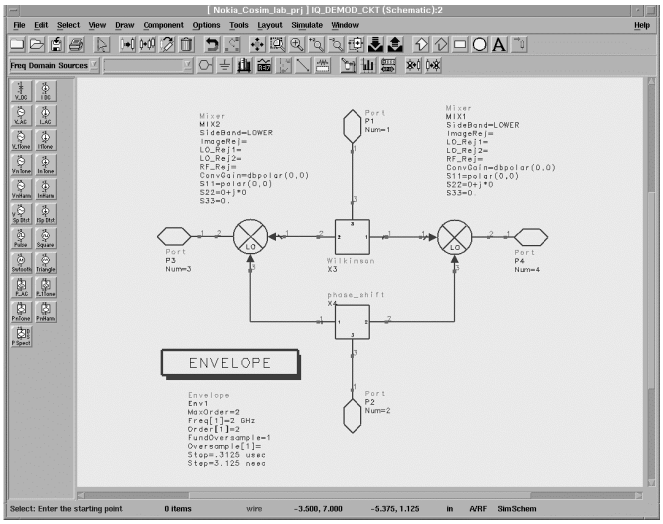
IQ Demodulator



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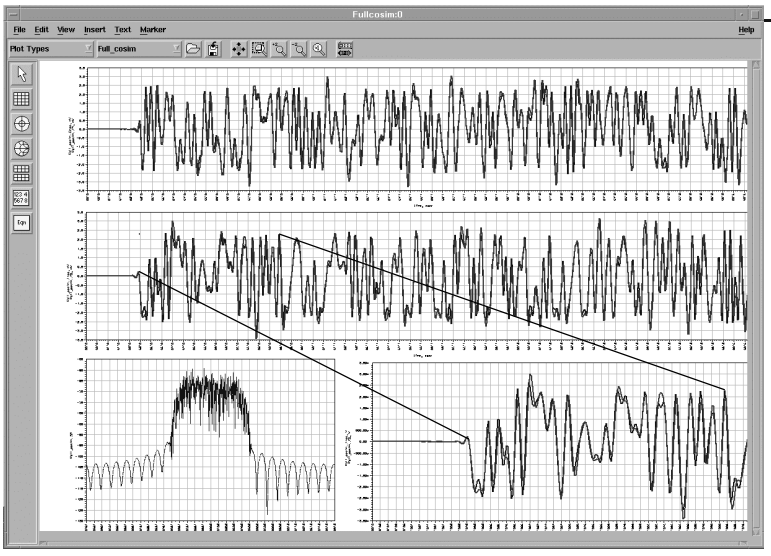
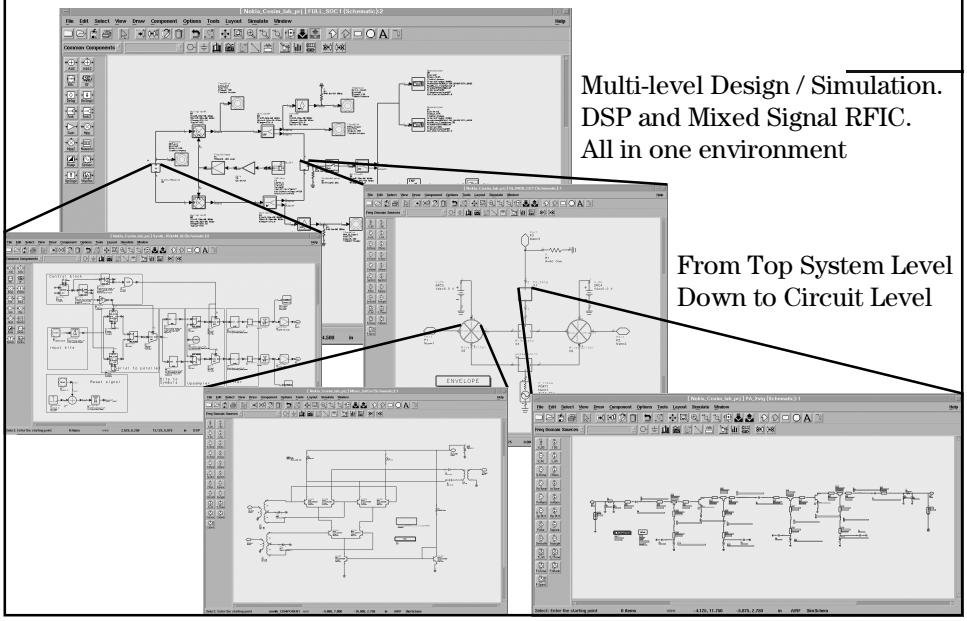
Typical 16 QAM, input and output recovered Data



Conclusion



Multi-level Design / Simulation.
DSP and Mixed Signal RFIC.
All in one environment

From Top System Level
Down to Circuit Level

Sources of additional information

- For more information on HP EEsof
  - http://www.hp.com/go/hpeesof
- For information on HP test and measurement equipment
  - http://www.tmo.hp.com/
- For more information on UC Berkeley Ptolemy:
  - http://ptolemy.eecs.berkeley.edu/

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