A-priori Node Assignment," *VLSI Signal Processing VII*, IEEE Press, 1994.

[Zivo95]

V. Zivojnovic, J. M. Velarde, C. Schlager and H. Meyer, "DSPSTONE: A DSP-Oriented Benchmarking Methodology," *Proceedings of ICSPAT*, 1995.

fied Framework, Ph. D. Thesis, Memorandum No. UCB/ERL M92/67, Electronics Research Laboratory, University of California, Berkeley, June 1992.

[Thor86]

Thor Tutorial, VLSI CAD Group, Stanford University, 1986.

[Vai93]

P. P. Vaidyanathan, *Multirate Systems and Filter Banks*, Prentice Hall, 1993.

[Veig90]

M. Veiga, J. Parera and J. Santos, "Programming DSP Systems on Multiprocessor Architectures," *Proceedings of the International Conference on Acoustics, Speech, and Signal Processing*, Albuquerque, April 1990.

[Yao93]

L. Yao and C. M. Woodside, "Iterative Decomposition and Aggregation of Stochastic Marked Graph Petri Nets," in *Advances in Petri Nets 1993*, pp. 325-349, edited by G. Rosenberg, Springer-Verlag, 1993.

[Zaky89]

A. Zaky and P. Sadayappan, "Optimal Static Scheduling of Sequential Loops on Multiprocessors," Proceedings of the *International Conference on Parallel Processing*, **Vol. 3**, pp. 130-137, 1989.

[Zivo94a]

V. Zivojnovic, S. Ritz and H. Meyr, "Retiming of DSP programs for optimum vectorization," *Proceedings of the International Conference on Acoustics, Speech, and Signal Processing*, April 1994.

[Zivo94b]

V. Zivojnovic, H. Koerner, and H. Meyr, "Multiprocessor Scheduling with

V. Sarkar, "Partitioning and Scheduling Parallel Programs for Multiprocessors," *Research Monographs in Parallel and Distributed Computing*, Pitman, London, 1989.

[Sha89]

P. L. Shaffer, "Minimization of Interprocessor Synchronization in Multiprocessors with Shared and Private Memory," *International Conference on Parallel Processing*, 1989.

[Schw85]

D. A. Schwartz, and T. P. Barnwell III, "Cyclo-Static Solutions: Optimal Multiprocessor Realizations of Recursive Algorithms," *VLSI Signal Processing II,* IEEE Special Publications, pp. 117-128, June 1985.

[Shen92]

N. Shenoy, R. K. Brayton, A. L. Sangiovanni-Vincentelli, "Graph algorithms for clock schedule optimization," in *1992 IEEE/ACM International Conference on Computer-Aided Design. Digest of Technical Papers* (Cat. No.92CH03183-1), Santa Clara, CA, pp. 132-6.

[Sih91]

G. C. Sih, *Multiprocessor Scheduling to account for Interprocessor Communication*, Ph. D. Thesis, Department of EECS, University of California Berkeley, April 1991.

[Stolz91]

A. Stolzle, *A Real Time Large Vocabulary Connected Speech Recognition System*, Ph. D. Thesis, Department of EECS, University of California Berkeley, December 1991.

[Sriv92]

M. B. Srivastava, *Rapid-Prototyping of Hardware and Software in a Uni-*

Vol. 8, No. 2, pp. 40-51, June 1991.

[Rajs94]

Sergio Rajsbaum and Mosha Sidi, "On the Performance of Synchronized Programs in Distributed Networks with Random Processing Times and Transmission Delays," *IEEE Transactions on Parallel and Distributed Systems*. **Vol. 5, No. 9**, September 1994.

[Ram80]

C. V. Ramamoorthy and G. S. Ho, "Performance Evaluation of Asynchronous Concurrent Systems using Petri Nets," *IEEE Transactions on Software Engineering*, **Vol. SE-6, No. 5**, pp. 440-449, September 1980.

[Ram72]

C. V. Ramamoorthy, K. M. Chandy, and M. J. Gonzalez, "Optimal Scheduling Strategies in Multiprocessor Systems," *IEEE Transactions on Computers*, Feb. 1972.

[Reit68]

R. Reiter, "Scheduling Parallel Computations", *Journal of the Association for Computing Machinery*, October 1968.

[Renf81]

M. Renfors and Y. Neuvo, "The Maximum Sampling Rate of Digital Filters Under Hardware Speed Constraints," *IEEE Transactions on Circuits and Systems*, **CAS-28(3)**, March 1981.

[Ritz92]

S. Ritz, M. Pankert, and H. Meyr, "High Level Software Synthesis for Signal Processing Systems," *Proceedings of the International Conference on Application Specific Array Processors*, Berkeley, August, 1992.

[Sark89]

J. Pino, S. Ha, E. A. Lee, and J. T. Buck, "Software Synthesis for DSP Using Ptolemy," *Journal of VLSI Signal Processing*, **Vol. 9**, **No. 1**, January, 1995.

[Pin95b]

J. L. Pino, S. S. Bhattacharyya and E. A. Lee, "A Hierarchical Multiprocessor Scheduling System for DSP Applications," to appear in *IEEE Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, CA, October 29 - November 1, 1995.

[Pow92]

D. B. Powell, E. A. Lee, and W. C. Newman, "Direct Synthesis of Optimized DSP Assembly Code from Signal Flow Block Diagrams," *Proceedings of the International Conference on Acoustics, Speech, and Signal Processing*, San Francisco, March, 1992.

[Prin91]

H. Printz, *Automatic Mapping of Large Signal Processing Systems to a Parallel Machine*, Ph.D. thesis, Memorandum CMU-CS-91-101, School of Computer Science, Carnegie Mellon University, May, 1991.

[Prin92]

H. Printz, "Compilation of Narrowband Spectral Detection Systems for Linear MIMD Machines," *Proceedings of the International Conference on Application Specific Array Processors*, Berkeley, August, 1992.

[Ptol94]

Ptolemy design group, UC Berkeley, *The Almagest*, UC Berkeley, 1994.

[Rab91]

J. M. Rabaey, C. Chu, P. Hoang, and M. Potkonjak, "Fast Prototyping of Datapath Intensive Architectures," *IEEE Design and Test of Computers*,

G. J. Olsder, J. A. C. Resing, R. E. De Vries and M. S. Keane, "Discrete Event Systems with Stochastic Processing Times," *IEEE Transactions on Automatic Control*, March 1990, **Vol.35**, No.3, pp. 299-302.

[Ols89]

G. J. Oldser, "Performance Analysis of Data-driven Networks," *Systolic Array Processors*; Contributions by Speakers at the International Conference on Systolic Arrays; Edited by: J. McCanny, J. McWhiter, E. Swartzlander Jr., Prentice Hall, New York, 1989, pp. 33-41.

[Ous94]

J. K. Ousterhout, *An Introduction to Tcl and Tk*, Addison-Wesley Publishing, Redwood City, CA, 1994.

[Pap90]

G. M. Papadopoulos, "Monsoon: A Dataflow Computing Architecture Suitable for Intelligent Control," *Proceedings of the 5th IEEE International Symposium on Intelligent Control*, 1990.

[Parhi91]

K. Parhi, and D. G. Messerschmitt, "Static Rate-optimal Scheduling of Iterative Data-flow Programs via Optimum Unfolding," *IEEE Transactions on Computers*, **Vol. 40, No. 2**, pp. 178-194, February 1991.

[Patt90]

D. A. Patterson and J. L. Hennessy, *Computer Architecture: A Quantitative Approach*, Morgan Kaufman Publishers, 1990.

[Peter81]

J. L. Peterson, *Petri Net Theory and the Modelling of Systems*, Prentice-Hall Inc., 1981.

[Pin95a]

32nd Design Automation Conference, June 1995.

[Li95]

Y. S. Li and S. Malik, "Performance Analysis of Embedded Software Using Implicit Path Enumeration," *Proceedings of the 32nd Design Automation Conference*, June 1995.

[Messer88]

D. G. Messerschmitt, "Breaking the Recursive Bottleneck," in *Performance Limits in Communication Theory and Practice*, J. K. Skwirzynski editor, Chapter 7, Kluwer Academic Publishers, 1988.

[Moll82]

Michael K. Molloy, "Performance Analysis Using Stochastic Petri Nets," *IEEE Transactions on Computers*, **Vol. c-31, No. 9**, September 1982.

[Moto89]

DSP96002 IEEE Floating-Point Dual-Port Processor User's Manual, Motorola Inc., 1989.

[Moto90]

DSP96000ADS Application Development System Reference Manual, Motorola Inc., 1990.

[Mouss92]

F. Moussavi and D. G. Messerschmitt, "Statistical Memory Management for Digital Signal Processing," *Proceedings of the 1992 IEEE International Symposium on Circuits and Systems*, **Vol. 2**, pp. 1011-14, May 1992.

[Mur89]

T. Murata, "Petri nets: Properties, Analysis, and Applications," *Proceedings of the IEEE*, **Vol. 77**, pp. 39-58, January 1989.

[Ols90]

E. A. Lee, "Consistency in Dataflow Graphs", *IEEE Transactions on Parallel and Distributed Systems*, Vol. 2, No. 2, April 1991.

[Lee93]

E. A. Lee, "Representing and Exploiting Data Parallelism Using Multidimensional Dataflow Diagrams," *Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing*, Minneapolis, **Vol. 1**, pp. 453-456, April 1993.

[Lee95]

E. A. Lee and T. M. Parks, "Dataflow Process Networks," *Proceedings of the IEEE*, May 1995.

[Lei91]

C. E. Leiserson and J. B. Saxe, "Retiming Synchronous Circuitry," *Algorithmica*, **Vol. 6**, **No. 1**, pp. 5-35, 1991.

[Len92]

D. Lenoski, J. Laudon, K. Gharachorloo, W. D. Weber and J. Hennessey, "The Stanford Dash multiprocessor," *IEEE Computer*, March 1992.

[Lew81]

H. R. Lewis and C. H. Papadimitriou, *Elements of the Theory of Computation*, Prentice Hall, 1982.

[Liao94]

G. Liao, G. R. Gao, E. Altman, and V. K. Agarwal, *A Comparative Study of DSP Multiprocessor List Scheduling Heuristics*, technical report, School of Computer Science, McGill University, 1994.

[Liao95]

S. Liao, S. Devadas, K. Keutzer, S. Tjiang and A. Wang, "Code Optimization Techniques for Embedded DSP Microprocessors," *Proceedings of the*

[Law76]

E. L. Lawler, *Combinatorial Optimization: Networks and Matroids*, Holt, Rinehart and Winston, New York, pp. 65-80, 1976.

[Lee86]

E. A. Lee, *A Coupled Hardware and Software Architecture for Programmable DSPs*, Ph. D. Thesis, Department of EECS, University of California Berkeley, May 1986.

[Lee87]

E. A. Lee and D. G. Messerschmitt, "Static Scheduling of Synchronous Dataflow Programs for Digital Signal Processing," *IEEE Transactions on Computers*, February, 1987.

[Lee88a]

E. A. Lee, "Programmable DSP Architectures, Part I", *IEEE Acoustics, Speech, and Signal Processing Magazine*, October, 1988.

[Lee88b]

E. A. Lee, "Recurrences, Iteration, and Conditionals in Statically Scheduled Block Diagram Languages," *VLSI Signal Processing III*, IEEE, Press, 1988.

[Lee89]

E. A. Lee, and S. Ha, "Scheduling Strategies for Multiprocessor Real-Time DSP," *Globecom*, Dallas Texas, pp. 1279-1283, November 1989.

[Lee90]

E. A. Lee and J. C. Bier, "Architectures for Statically Scheduled Dataflow," *Journal of Parallel and Distributed Computing*, **Vol. 10**, pp. 333-348, December 1990.

[Lee91]

Computers, pp. 1235-1238, December 1975.

[Kung87]

S. Y. Kung, P. S. Lewis, and S. C. Lo, "Performance Analysis and Optimization of VLSI Dataflow Arrays" *Journal of Parallel and Distributed Computing,* **Vol. 4**, pp. 592-618, 1987.

[Kung88]

S. Y. Kung, *VLSI array processors*, Englewood Cliffs, N. J., Prentice Hall, 1988.

[Lam88]

M. Lam, "Software Pipelining: An Effective Scheduling Technique for VLIW Machines," *Proceedings of the SIGPLAN 1988 Conference on Programming Language Design and Implementation,* pp. 318-328, June 1988.

[Lam89]

M. Lam, *A Systolic Array Optimizing Compiler*, Kluwer Academic Publishers, Norwell, Massachusetts, 1989.

[Lamp86]

L. Lamport, "The Mutual Exclusion Problem: Part I and II," *Journal of the ACM*, **Vol. 33, No. 2**, pp. 313-348, April 1986.

[Laps91]

P. D. Lapsley, *Host Interface and Debugging of Dataflow DSP Systems*, M. S. Thesis, Electronics Research Laboratory, University of California, Berkeley, CA 94720, December, 1991.

[Lauw90]

R. Lauwereins, M. Engels, J.A. Peperstraete, E. Steegmans, and J. Van Ginderdeuren, "GRAPE: A CASE Tool for Digital Signal Parallel Processing," *IEEE ASSP Magazine*, **Vol. 7, No. 2**, April, 1990.

185, 1991.

[Hu61]

T. C. Hu, "Parallel Sequencing and Assembly Line Problems," *Operations Research*, **Vol. 9**, 1961.

[Huis93]

J. A. Huisken et. al., "Synthesis of Synchronous Communication Hardware in a Multiprocessor Architecture," *Journal of VLSI Signal Processing*, **Vol. 6**, pp.289-299, 1993.

[Kala93]

A. Kalavade, and E. A. Lee, "A Hardware/Software Codesign Methodology for DSP Applications," *IEEE Design and Test*, September 1993, **Vol. 10, No. 3**, pp. 16-28.

[Karp66]

R. M. Karp and R. E. Miller, "Properties of a Model for Parallel Computations: Determinacy, Termination Queueing," *SIAM Journal of Applied Math.*, **Vol. 14**, **No. 6**, November, 1966.

[Karp78]

R. M. Karp, "A Characterization of the Minimum Cycle Mean in a Digraph," *Discrete Mathematics*, **Vol. 23**, 1978.

[Koh90]

W. Koh, *A Reconfigurable Multiprocessor System for DSP Behavioral Simulation*, Ph. D. Thesis, Memorandum No. UCB/ERL M90/53, Electronics Research Laboratory, University of California, Berkeley, June 1990.

[Koh75]

W. H. Kohler, "A Preliminary Evaluation of Critical Path Method for Scheduling Tasks on Multiprocessor Systems," *IEEE Transactions on*

[Gau91]

J. Gaudiot and L. Bic, *Advanced Topics in Data-flow Computing*, Prentice Hall, Englewood Cliffs, New Jersey, 1991.

[Gov94]

R. Govindarajan, G. R. Gao, and P. Desai, "Minimizing Memory Requirements in Rate-Optimal Schedules," *Proceedings of the International Conference on Application Specific Array Processors*, San Francisco, August, 1994.

[Grin88]

C. M. Grinstead, "Cycle Lengths in $A^k b^*$," *SIAM Journal on Matrix Analysis*, October 1988.

[Ha92]

S. Ha, *Compile Time Scheduling of Dataflow Program Graphs with Dynamic Constructs*, Ph. D. Thesis, Memorandum No. UCB/ERL M92/43, April 1992.

[Hal91]

N. Halbwachs, P. Caspi, P. Raymond and D. Pilaud, "The Synchronous Data Flow Programming Language LUSTRE," *Proceedings of the IEEE*, September 1991.

[Hal93]

N. Halbwachs, *Synchronous Programming of Reactive Systems*, Kluwer Academic Publishers, 1993.

[Hav91]

B. R. Haverkort, "Approximate Performability Analysis Using Generalized Stochastic Petri Nets," *Proceedings of the Fourth International Workshop on Petri Nets and Performance Models*, Melbourne, Australia, pp. 176-

G. De Micheli, *Synthesis and Optimization of Digital Circuits*, McGraw Hill Inc., New Jersey, 1994.

[Denn80]

J. B. Dennis, "Dataflow Supercomputers," *IEEE Computer Magazine*, **Vol. 13, No. 11**, November, 1980.

[Dietz92]

H. G. Dietz, A. Zaafrani, and M. T. O'Keefe, "Static Scheduling for Barrier MIMD Architectures," *Journal of Supercomputing*, **Vol. 5**, **No. 4**, 1992.

[Durr91]

R. Durett, *Probability: Theory and Examples*, Wadsworth & Brooks/Cole Statistics/Probability Series, Pacific Grove, CA, 1991.

[Filo93]

D. Filo, D. C. Ku, C. N. Coelho Jr., and G. De Micheli, "Interface Optimization for Concurrent Systems Under Timing Constraints," *IEEE Transactions on Very Large Scale Integration*, **Vol. 1**, **No. 3**, September, 1993.

[Gajs94]

D. J. Gajski, F. Vahid, S. Narayan and J. Gong, *Specification and Design of Embedded Systems*, Prentice Hall, Englewood Cliffs, New Jersey, 1994.

[Garey79]

M. R. Garey and D. S. Johnson, *Computers and Intractability — A Guide to the Theory of NP-Completeness*, W. H. Freeman and Company, New York, 1979.

[Gasp92]

F. Gasperoni and Uwe Schweigelshohn, "Scheduling Loops on Parallel Processors: A Simple Algorithm with Close to Optimum Performance," *International Conference on Vector & Parallel Processors*, Sept. 1992.

ing: The NEC mPD7281," *IEEE Workshop on Signal Processing*, November 1984.

[Chao92]

L. F. Chao, and E. Sha, "Unfolding and Retiming Data-Flow DSP Programs for RISC Multiprocessor Scheduling," *Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing*, April 1992.

[Chre83]

P. Chretienne, "Timed Event Graphs: A Complete Study of their Controlled Executions," *International Workshop on Timed Petri Nets*, July 1985.

[Cohen85]

G. Cohen, D. Dubois, J. Quadrat, "A Linear System Theoretic View of Discrete Event Processes and its use for Performance Evaluation in Manufacturing," *IEEE Transactions on Automatic Control*, March 1985.

[Corm92]

T. H. Cormen, C. E. Leiserson, and R. L. Rivest, *Introduction to Algorithms*, The MIT Press and the McGraw Hill Book Company, Sixth printing, Chapter 25, pp. 542-543, 1992.

[Cun79]

R. Cunningham-Green, "Minimax Algebra," *Lecture Notes in Economics and Mathematical Systems,* **Vol. 166**, Springer-Verlag 1979.

[deGroot92]

S. M. H. de Groot, S. Gerez, and O. Herrmann, "Range-Chart-Guided Iterative Data-Flow Graph Scheduling," *IEEE Transactions on Circuits and Systems*, pp. 351-364, May 1992.

[DeMich94]

S. Borkar et. al., “iWarp: An Integrated Solution to High-Speed Parallel Computing”, *Proceedings of Supercomputing 1988 Conference*, Orlando, Florida, 1988.

[Bray84]

R. K. Brayton, G. D. Hachtel, C. T. McMullen, and A. L. Sangiovanni-Vincentelli, *Logic Minimization Algorithms for VLSI Synthesis*, Kluwer Academic Publishers, 1984.

[Bryant86]

R. E. Bryant, “Graph Based Algorithms for Boolean Function Manipulation,” *IEEE Transactions on Computers*, C-35(8), pp. 677-691, August 1986.

[Buck93]

J. T. Buck, *Scheduling Dynamic Dataflow Graphs with Bounded Memory using the Token Flow Model*, Ph. D. Thesis, Memorandum No. UCB/ERLM93/69, Electronics Research Laboratory, University of California at Berkeley, September, 1993.

[Buck94]

J. T. Buck, S. Ha, E. A. Lee, and D. G. Messerschmitt, “Ptolemy: A Framework for Simulating and Prototyping Heterogeneous Systems,” *International Journal of Computer Simulation*, January 1994.

[Cam92]

J. Campos and M. Silva, “Structural Techniques and Performance Bounds of Stochastic Petri Net Models,” in *Advances in Petri Nets 1993*, pp. 325-349, edited by G. Rosenberg, Springer-Verlag, 1993.

[Chase84]

M. Chase, “A Pipelined Data Flow Architecture for Digital Signal Process-

S. S. Bhattacharyya, S. Sriram, and E. A. Lee, *Resynchronization for Embedded Multiprocessors*, Draft XXX, to be made into an ERL memo.

[Bhat93]

S. S. Bhattacharyya and Edward A. Lee, "Scheduling Synchronous Dataflow Graphs for Efficient Looping," *Journal of VLSI Signal Processing*, **No. 6**, 1993.

[Bhat94]

S. S. Bhattacharyya and E. A. Lee, "Memory Management for Dataflow Programming of Multirate Signal Processing Algorithms," *IEEE Trans. on Signal Processing*, **Vol. 42, No. 5**, May 1994.

[Bier89]

J. Bier and E. A. Lee, "Frigg: A Simulation Environment for Multiprocessor DSP System Development", *Proceedings of the International Conference on Computer Design*, pp. 280-283, October, 1989, Boston, MA.

[Bier90]

J. Bier, S. Sriram and E. A. Lee, "A Class of Multiprocessor Architectures for Real-Time DSP," *VLSI DSP IV*, ed. H. Moscovitz, IEEE Press, November, 1990.

[Bils94]

G. Bilsen, M. Engels, R. Lauwereins and J. A. Peperstraete, "Static Scheduling of Multi-Rate and Cyclo-Static DSP Applications," *VLSI SIgnal Processing VII*, IEEE Press, 1994.

[Blaz87]

J. Blazewicz, "Selected Topics in Scheduling Theory," in *Surveys in Combinatorial Optimization*, North Holland Mathematica Studies, 1987.

[Bork88]

Dataflow Architecture," *IEEE Transactions on Computers*, **Vol. C-39, No. 3**, March, 1990.

[Arvi91]

Arvind, L. Bic, and T. Ungerer, "Evolution of Dataflow Computers," *Advanced Topics in Dataflow Computing*, Prentice-Hall, 1991.

[Bacc92]

F. Baccelli, G. Cohen, G. J. Olsder, and J.-P. Quadrat, *Synchronization and Linearity*, John Wiley & Sons Inc., New York, pp. 103-154, 1992.

[Bacc92]

F. Baccelli and Z. Liu, "On a Class of Stochastic Recursive Sequences Arising in Queueing Theory," *The Annals of Probability*, **Vol. 20, No. 1**, pp. 350-374.

[Barr91]

B. Barrera and E. A. Lee, "Multirate Signal Processing in Comdisco's SPW," *Proceedings of the International Conference on Acoustics, Speech, and Signal Processing*, Toronto, April, 1991.

[Ben91]

A. Benveniste and G. Berry, "The Synchronous Approach to Reactive and Real-Time Systems," *Proceedings of the IEEE*, **Vol. 79, No. 9**, 1991, pp.1270-1282.

[Bhat95a]

S. S. Bhattacharyya, S. Sriram, and E. A. Lee, *Optimizing Synchronization in Multiprocessor Implementations of Iterative Dataflow Programs*, ERL Technical Report UCB/ERL M95/2, University of California, Berkeley, CA 94720, January 5, 1995.

[Bhat95b]

REFERENCES

[Ack82]

W. B. Ackerman, "Data Flow Languages," *IEEE Computer Magazine*, **Vol. 15, No. 2**, February, 1982.

[Adam74]

T. L. Adam, K. M. Chandy and J. R. Dickson, "A Comparison of List Schedules for Parallel Processing Systems," *Communications of the ACM*, **Vol. 17, No. 12**, pp. 685-690, December 1974.

[Aik88]

A. Aiken, and A. Nicolau, "Optimal Loop Parallelization," *Proceedings of the SIGPLAN 88 Conference on Programming Language Design and Implementation*, 1988.

[Alle87]

R. Allen and K. Kennedy, "Automatic Transformation of Fortran Programs to Vector Form," *ACM Transactions on Programming Languages and Systems*, **Vol. 9, No. 4**, October, 1987.

[Ambl92]

A. L. Ambler, M. M. Burnett, and B. A. Zimmerman, "Operational Versus Definitional: A Perspective on Programming Paradigms," *IEEE Computer Magazine*, **Vol. 25, No. 9**, September, 1992.

[Ariel91]

User's Manual for the S-56X, Ariel Corporation, Highland Park, New Jersey, 1991.

[Arvi90]

Arvind and R. S. Nikhil, "Executing a Program on the MIT Tagged-Token